IMPACT: International Journal of Research in Engineering & Technology (IMPACT: IJRET)
ISSN(E): 2321-8843; ISSN(P): 2347-4599
Vol. 2, Issue 4, Apr 2014, 199-206

DESIGN OF PARALLEL PIPELINED FEED FORWARD ARCHITECTURE FOR ZERO FREQUENCY & MINIMUM COMPUTATION (ZMC) ALGORITHM OF FFT

K. JAYARAM[1], C. ARUN[2] & B. SAKTHIVEL[3]

[1,3]Assistant Professor, Department of ECE, Madurai Institute of Engineering & Technology, Tamil Nadu, India

[2]Professor, Department of ECE, R.M.K College of Engineering & Technology, Tamil Nadu, India

ABSTRACT

A new parallel pipelined feed forward architecture for real-time signal is proposed. A hardware oriented radix-2 algorithm is derived by integrating a twiddle factor decomposition technique in the divide and conquer approach. The butterfly structure of radix-2 algorithm is modified in accordance with the flow of signal. The new butterfly structures are designed to handle the hybrid data path which consists of real & complex data paths. The proposed approach which can be extended to all radix-2^k based DITFFT & DIFFFT algorithms. The zero frequency is computed without processing the zero input data. The symmetry property is applicable to minimize the stage computation in half of the actual stage. The proposed radix-2^k feed forward architectures need to use fewer hardware resources in hardware architecture. The proposed radix 2^k architectures lead to low hardware complexity with respect to adders and delays. The N-point 4-parallel radix-2^2 architecture requires $4(\log_{16}N-1)$ complex multipliers, $\log_2 N$ real adders and N-1 complex delay elements.

KEYWORDS: DITFFT & DIFFFT Algorithms, Fast Fourier Transform (FFT)